CLAIMS

What is claimed is:

1. A non-volatile memory device, comprising:
a memory cell; and

a plurality of sub-cells included in the memory cell and including at least one magneto resistive element;

wherein the sub-cells are electrically connected.

2. A memory device as in claim 1 wherein the sub-cells are connected in series.

3. A memory device as recited in claim 1 wherein the sub-cells are connectedin parallel.

4. A memory device as recited in claim 1 further comprising a transistor electrically connected with the magneto resistive element.

5. The non-volatile memory device according to Claim 1, wherein the sub-cell is composed of a plurality of sub-cells comprising a plurality of magneto resistive elements connected in parallel and one selection transistor connected with the magneto resistive elements and wherein the sub-cells are connected in series.

6. The non-volatile memory device according to Claim 1, wherein at least one sub-cell comprises a plurality of magneto resistive elements connected in series and one selection transistor, and wherein the memory cell comprises a plurality of sub-cells connected in parallel.

7. The non-volatile memory device according to Claim 1, wherein the sub-cell is composed of one magneto resistive element and one selection transistor, and wherein the memory cell comprises n_2 parallel sub-cells connected in series (n_2 is at least 2), the parallel sub-cell comprising the n_1 sub-cells connected in parallel (n_1 is at least 2).

8. A non-volatile memory device, comprising:
a memory cell, the memory cell further comprising:
a plurality of sub-cells connected in series; and
one selection transistor electrically connected with at least one of the sub-cells;
wherein the sub-cell comprises a plurality of magneto resistive elements connected in parallel with one another.

9. The non-volatile memory device according to claim 1, wherein the number of sub-cells in a memory cell equals the number of magneto resistive elements in a sub-cell.

10. The non-volatile memory device according to Claim 1, wherein the each mangetoresistive element includes a mangetically free layer and wherein writing of information into the memory cell is performed by magnetizing into the same direction the free layers of the magneto resistive elements included in the memory cell, and wherein the reading of the information recorded in the memory cell is performed by detecting the resistance value of the whole memory cell.

11. A non-volatile memory device, comprising:

a plurality of memory cells comprising a magneto resistive element and a selection transistor;

wherein the memory cells are arranged into a two dimensional

array;

a first interconnect line extending in a first direction of the memory array and functioning as a gate electrode of a selection transistor included in the memory cell;

a second interconnect line extending in a second direction of the memory array and connected to one end of the memory cell;

a third interconnect line extending in the second direction and connected to the other end of the memory cell;

where a circuit having the ends of the second and third interconnect lines as its terminals in a circuit region in the periphery of the memory array is connected in series with a circuit for another memory cell adjacent thereto in the first direction.

12. The non-volatile memory device according to Claim 11, wherein the writing of one bit of information into the non-volatile memory device is performed by magnetizing into the same direction the free layers of the magneto resistive elements of a plurality of the memory cells which are formed at the positions of intersection of a plurality of the first interconnect lines and a plurality of the second interconnect lines, and wherein the reading of one bit of information from the non-volatile memory device is performed by inputting the same read control signal to the plurality of the first interconnect lines and detecting the resistance value between the second interconnection line and the third interconnection line of the circuits connected in series.

13. The non-volatile memory device according to Claim 12, wherein the number of the plurality of the first interconnect

lines is the same as the number of the circuits connected in series.

14. A memory device, comprising:

a plurality of electrically connected memory cells, each memory cell comprising:

a plurality of sub-cells electrically connected with one another, each sub cell further comprising:

a magnetoresistive device, and

a transistor electrically connected with the magnetoresitive device.

15. A memory device as recited in claim 14, further comprising: a sub-cell including a plurality of magnetoresistive devices conected in parallel with one another.